

The listing of claims will replace all prior versions, and listings, of claims in the application:

**Listing of Claims:**

1. (Currently Amended) A semiconductor device comprising:  
a pixel portion comprising a plurality of pixels;  
a first circuit; and  
a second circuit,  
wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,  
wherein the first circuit is configured to output a timing signal to the second circuit, and  
wherein the second circuit is configured to select either only one of the sensor portion and the liquid crystal element portion, and output a pulse signal based on the timing signal to the selected one of the sensor portion and the liquid crystal element portion.
  
2. (Currently Amended) A semiconductor device comprising:  
a pixel portion comprising a plurality of pixels;  
a first circuit; and  
a second circuit,  
wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,  
wherein the second circuit comprises a first logical circuit and a second logical circuit,  
wherein the first circuit is configured to output a timing signal to the first logical circuit and to the second logical circuit,

wherein the first logical circuit is electrically connected to the sensor portion, and the second logical circuit is electrically connected to the light emitting element portion,

wherein the second circuit is so configured that either only one of the first logical circuit and the second logical circuit outputs a pulse signal based on the timing signal to the pixel portion, and

wherein the pulse signal output from the first logical circuit is different from the pulse signal output from the second logical circuit.

3. (Currently Amended) A semiconductor device comprising:

a pixel portion comprising a plurality of pixels;

a first circuit; and

a second circuit,

wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,

wherein the second circuit comprises a first logical circuit and a second logical circuit,

wherein the first circuit is configured to output a timing signal to the first logical circuit and to the second logical circuit,

wherein the first logical circuit is electrically connected to the sensor portion, and the second logical circuit is electrically connected to the liquid crystal element portion,

wherein the second circuit is so configured that either only one of the first logical circuit and the second logical circuit outputs a pulse signal based on the timing signal to the pixel portion, and

wherein the pulse signal output from the first logical circuit is different from the pulse signal output from the second logical circuit.

4. (Currently Amended) A semiconductor device comprising:

a pixel portion comprising a plurality of pixels;

a first circuit; and  
a second circuit,  
wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,  
wherein the sensor portion comprises a first TFT, and the light emitting element portion comprises a second TFT,  
wherein the second circuit comprises a first logical circuit and a second logical circuit;  
wherein a gate of the first TFT is electrically connected to the first logical circuit, and a gate of the second TFT is electrically connected to the second logical circuit,  
wherein the first circuit is configured to output a timing signal to the first logical circuit and to the second logical circuit,  
wherein the second circuit is so configured that either only one of the first logical circuit and the second logical circuit outputs a pulse signal based on the timing signal to the pixel portion, and  
wherein the pulse signal output from the first logical circuit is different from the pulse signal output from the second logical circuit.

5. (Currently Amended) A semiconductor device comprising:  
a pixel portion comprising a plurality of pixels;  
a first circuit; and  
a second circuit,  
wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,  
wherein the sensor portion comprises a first TFT, and the liquid crystal element portion comprises a second TFT,  
wherein the second circuit comprises a first logical circuit and a second logical circuit;

wherein a gate of the first TFT is electrically connected to the first logical circuit, and a gate of the second TFT is electrically connected to the second logical circuit,

wherein the first circuit is configured to output a timing signal to the first logical circuit and to the second logical circuit,

wherein the second circuit is so configured that ~~either~~ only one of the first logical circuit and the second logical circuit outputs a pulse signal based on the timing signal to the pixel portion, and

wherein the pulse signal output from the first logical circuit is different from the pulse signal output from the second logical circuit.

6. (Currently Amended) A semiconductor device comprising:

a pixel portion having a plurality of pixels;

a first circuit; and

a second circuit,

wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,

wherein the sensor portion comprises a first TFT, and the light emitting element portion comprises a second TFT,

wherein the second circuit comprises a first logical circuit and a second logical circuit,

wherein the first circuit is configured to output a timing signal to the first logical circuit and to the second logical circuit,

wherein an image signal generated by the sensor portion is input to the light emitting element portion, and

wherein the second circuit is so configured that, when only one of the first logical circuit and the second logical circuit outputs a non-selection signal to one of the first TFT and the second TFT, the other of the first logical circuit and the second logical

circuit outputs a selection signal based on the timing signal to the other of the first TFT and the second TFT.

7. (Currently Amended) A semiconductor device comprising:  
a pixel portion comprising a plurality of pixels;  
a first circuit comprising a shift register;  
a second circuit; and  
one of a back light and a front light,  
wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,  
wherein the sensor portion comprises a first TFT, and the liquid crystal element portion comprises a second TFT,  
wherein the second circuit comprises a first logical circuit and a second logical circuit,  
wherein a first signal line is electrically connected to the first logical circuit, and a second signal line is electrically connected to the second logical circuit,  
wherein the first TFT is electrically connected to the first signal line, and the second TFT is electrically connected to the second signal line,  
wherein the first circuit is configured to output a timing signal based on an output signal of the shift register to the first logical circuit and to the second logical circuit,  
wherein an image signal generated by the sensor portion is input to the liquid crystal element portion,  
wherein the second circuit is so configured that, when only one of the first logical circuit and the second logical circuit outputs a non-selection signal to one of the first TFT and the second TFT, the other of the first logical circuit and the second logical circuit outputs a selection signal based on the timing signal to the other of the first TFT and the second TFT.

8. (Original) A semiconductor device according to claim 2, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

9. (Original) A semiconductor device according to claim 3, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

10. (Original) A semiconductor device according to claim 4, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

11. (Previously Presented) A semiconductor device according to claim 5, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

12. (Original) A semiconductor device according to claim 6, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

13. (Original) A semiconductor device according to claim 7, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

14. (Original) A semiconductor device according to claim 2, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

15. (Original) A semiconductor device according to claim 3, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

16. (Original) A semiconductor device according to claim 4, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

17. (Original) A semiconductor device according to claim 5, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

18. (Original) A semiconductor device according to claim 6, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

19. (Original) A semiconductor device according to claim 7, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

20. (Original) A semiconductor device according to claim 2, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

21. (Original) A semiconductor device according to claim 3, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

22. (Original) A semiconductor device according to claim 4, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

23. (Original) A semiconductor device according to claim 5, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

24. (Original) A semiconductor device according to claim 6, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

25. (Original) A semiconductor device according to claim 7, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

26. (Original) A semiconductor device according to claim 2, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

27. (Original) A semiconductor device according to claim 3, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

28. (Original) A semiconductor device according to claim 4, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

29. (Original) A semiconductor device according to claim 5, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

30. (Original) A semiconductor device according to claim 6, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

31. (Original) A semiconductor device according to claim 7, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

32. (Previously Presented) A semiconductor device according to claim 6, wherein the first logical circuit is electrically connected to the first TFT through a first signal line,

wherein the second logical circuit is electrically connected to the second TFT through a second signal line, and

wherein the second signal line is a selection signal line, and the first signal line is a sensor selection signal line.

33. (Previously Presented) A semiconductor device according to claim 6, wherein the first logical circuit is electrically connected to the first TFT through a first signal line,

wherein the second logical circuit is electrically connected to the second TFT through a second signal line, and

wherein the second signal line is a reset signal line, and the first signal line is a sensor reset signal line.

34. (Previously Presented) A semiconductor device according to claim 6,  
wherein the first logical circuit is electrically connected to the first TFT through a  
first signal line,

wherein the second logical circuit is electrically connected to the second TFT  
through a second signal line, and

wherein the second signal line is a selection signal line, and the first signal line is  
a sensor reset signal line.

35. (Previously Presented) A semiconductor device according to claim 6,  
wherein the first logical circuit is electrically connected to the first TFT through a  
first signal line,

wherein the second logical circuit is electrically connected to the second TFT  
through a second signal line, and

wherein the second signal line is a reset signal line, and the first signal line is a  
sensor selection signal line.

36. (Original) A semiconductor device according to claim 7, wherein one of the  
first signal line and the second signal line is a liquid crystal selection signal line, and the  
other is a sensor selection signal line.

37. (Original) A semiconductor device according to claim 7, wherein one of the  
first signal line and the second signal line is a liquid crystal selection signal line, and the  
other is a sensor reset signal line.

38. (Original) A semiconductor device according to claim 4, wherein one of the  
first TFT and the second TFT is a selection TFT, and the other is a sensor selection  
TFT.

39. (Original) A semiconductor device according to claim 6, wherein one of the first TFT and the second TFT is a selection TFT, and the other is a sensor selection TFT.

40. (Original) A semiconductor device according to claim 4, wherein one of the first TFT and the second TFT is a selection TFT, and the other is a sensor reset TFT.

41. (Original) A semiconductor device according to claim 6, wherein one of the first TFT and the second TFT is a selection TFT, and the other is a sensor reset TFT.

42. (Original) A semiconductor device according to claim 4, wherein one of the first TFT and the second TFT is a reset TFT, and the other is a sensor reset TFT.

43. (Original) A semiconductor device according to claim 6, wherein one of the first TFT and the second TFT is a reset TFT, and the other is a sensor reset TFT.

44. (Original) A semiconductor device according to claim 4, wherein one of the first TFT and the second TFT is a reset TFT, and the other is a sensor selection TFT.

45. (Original) A semiconductor device according to claim 6, wherein one of the first TFT and the second TFT is a reset TFT, and the other is a sensor selection TFT.

46. (Original) A semiconductor device according to claim 5, wherein one of the first TFT and the second TFT is a liquid crystal selection TFT, and the other is a sensor selection TFT.

47. (Original) A semiconductor device according to claim 7, wherein one of the first TFT and the second TFT is a liquid crystal selection TFT, and the other is a sensor selection TFT.

48. (Original) A semiconductor device according to claim 5, wherein one of the first TFT and the second TFT is a liquid crystal selection TFT, and the other one is a sensor reset TFT.

49. (Original) A semiconductor device according to claim 7, wherein one of the first TFT and the second TFT is a liquid crystal selection TFT, and the other is a sensor reset TFT.

50. (Previously Presented) A semiconductor device according to claim 2, wherein an output terminal of the first logical circuit is electrically connected to at least one inverter circuit.

51. (Previously Presented) A semiconductor device according to claim 3, wherein an output terminal of the first logical circuit is electrically connected to at least one inverter circuit.

52. (Previously Presented) A semiconductor device according to claim 4, wherein an output terminal of the first logical circuit is electrically connected to at least one inverter circuit.

53. (Previously Presented) A semiconductor device according to claim 5, wherein an output terminal of the first logical circuit is electrically connected to at least one inverter circuit.

54. (Previously Presented) A semiconductor device according to claim 6, wherein an output terminal of the first logical circuit is electrically connected to at least one inverter circuit.

55. (Previously Presented) A semiconductor device according to claim 7, wherein an output terminal of the first logical circuit is electrically connected to at least one inverter circuit.

56. (Previously Presented) A semiconductor device according to claim 2, wherein an output terminal of the second logical circuit is electrically connected to at least one inverter circuit.

57. (Previously Presented) A semiconductor device according to claim 3, wherein an output terminal of the second logical circuit is electrically connected to at least one inverter circuit.

58. (Previously Presented) A semiconductor device according to claim 4, wherein an output terminal of the second logical circuit is electrically connected to at least one inverter circuit.

59. (Previously Presented) A semiconductor device according to claim 5, wherein an output terminal of the second logical circuit is electrically connected to at least one inverter circuit.

60. (Previously Presented) A semiconductor device according to claim 6, wherein an output terminal of the second logical circuit is electrically connected to at least one inverter circuit.

61. (Previously Presented) A semiconductor device according to claim 7, wherein an output terminal of the second logical circuit is electrically connected to at least one inverter circuit.

62. (Original) A semiconductor device according to claim 2, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a reset TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

63. (Original) A semiconductor device according to claim 4, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a reset TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

64. (Original) A semiconductor device according to claim 6, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a reset TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

65. (Original) A semiconductor device according to claim 2 wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

66. (Original) A semiconductor device according to claim 4, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

67. (Original) A semiconductor device according to claim 6, wherein each of the plurality of pixels comprises a light emitting element, a selection TFT, a driver TFT, a

photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

68. (Previously Presented) A semiconductor device according to claim 1, wherein each of the plurality of pixels comprises a liquid crystal element, a liquid crystal selection TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

69. (Previously Presented) A semiconductor device according to claim 3, wherein each of the plurality of pixels comprises a liquid crystal element, a liquid crystal selection TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

70. (Previously Presented) A semiconductor device according to claim 5, wherein each of the plurality of pixels comprises a liquid crystal element, a liquid crystal selection TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

71. (Previously Presented) A semiconductor device according to claim 7, wherein each of the plurality of pixels comprises a liquid crystal element, a liquid crystal selection TFT, a photoelectric conversion element, a sensor selection TFT, a sensor driver TFT, and a sensor reset TFT.

72. (Original) A semiconductor device according to claim 1, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

73. (Original) A semiconductor device according to claim 2, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

74. (Original) A semiconductor device according to claim 3, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

75. (Original) A semiconductor device according to claim 4, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

76. (Original) A semiconductor device according to claim 5, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

77. (Original) A semiconductor device according to claim 6, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

78. (Original) A semiconductor device according to claim 7, wherein each of the plurality of pixels comprises three light emitting elements and one photoelectric conversion element.

79. (Original) A display device using a semiconductor device according to claim 1.

2. 80. (Original) A display device using a semiconductor device according to claim
3. 81. (Original) A display device using a semiconductor device according to claim
4. 82. (Original) A display device using a semiconductor device according to claim
5. 83. (Original) A display device using a semiconductor device according to claim
6. 84. (Original) A display device using a semiconductor device according to claim
7. 85. (Original) A display device using a semiconductor device according to claim
86. (Original) A scanner using a semiconductor device according to claim 1.
87. (Original) A scanner using a semiconductor device according to claim 2.
88. (Original) A scanner using a semiconductor device according to claim 3.
89. (Original) A scanner using a semiconductor device according to claim 4.
90. (Original) A scanner using a semiconductor device according to claim 5.

91. (Original) A scanner using a semiconductor device according to claim 6.
92. (Original) A scanner using a semiconductor device according to claim 7.
93. (Original) A portable information terminal using a semiconductor device according to claim 1.
94. (Original) A portable information terminal using a semiconductor device according to claim 2.
95. (Original) A portable information terminal using a semiconductor device according to claim 3.
96. (Original) A portable information terminal using a semiconductor device according to claim 4.
97. (Original) A portable information terminal using a semiconductor device according to claim 5.
98. (Original) A portable information terminal using a semiconductor device according to claim 6.
99. (Original) A portable information terminal using a semiconductor device according to claim 7.
100. (Currently Amended) A semiconductor device comprising:  
a pixel portion comprising a plurality of pixels;  
a first circuit; and

a second circuit,  
wherein each of the plurality of pixels comprises a sensor portion and a light emitting element portion,  
wherein the first circuit is configured to output a timing signal to the second circuit,  
wherein the second circuit is electrically connected to the sensor portion and to the light emitting element portion, and  
wherein the second circuit is configured to select either only one of the sensor portion and the light emitting element portion depending on a control signal, and output a pulse signal based on the timing signal to the selected one of the sensor portion and the light emitting element portion.

101. (Currently Amended) A semiconductor device comprising:  
a pixel portion comprising a plurality of pixels;  
a first circuit; and  
a second circuit,  
wherein each of the plurality of pixels comprises a sensor portion and a liquid crystal element portion,  
wherein the first circuit is configured to output a timing signal to the second circuit,  
wherein the second circuit is electrically connected to the sensor portion and to the liquid crystal element portion, and  
wherein the second circuit is configured to select either only one of the sensor portion and the liquid crystal element portion depending on a control signal, and output a pulse signal based on the timing signal to the selected one of the sensor portion and the liquid crystal element portion.

102. (Previously Presented) A semiconductor device according to claim 100, wherein the second circuit comprises a first logical circuit and a second logical circuit, and the first logical circuit is electrically connected to the sensor portion and the second logical circuit is electrically connected to the light emitting element portion.

103. (Previously Presented) A semiconductor device according to claim 101, wherein the second circuit comprises a first logical circuit and a second logical circuit, and the first logical circuit is electrically connected to the sensor portion and the second logical circuit is electrically connected to the liquid crystal element portion.

104. (Previously Presented) A semiconductor device according to claim 102, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

105. (Previously Presented) A semiconductor device according to claim 103, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is a NOR circuit.

106. (Previously Presented) A semiconductor device according to claim 102, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

107. (Previously Presented) A semiconductor device according to claim 103, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is a NOR circuit.

108. (Previously Presented) A semiconductor device according to claim 102, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

109. (Previously Presented) A semiconductor device according to claim 103, wherein one of the first logical circuit and the second logical circuit is a NAND circuit and the other is an OR circuit.

110. (Previously Presented) A semiconductor device according to claim 102, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

111. (Previously Presented) A semiconductor device according to claim 103, wherein one of the first logical circuit and the second logical circuit is an AND circuit and the other is an OR circuit.

112. (Previously Presented) A semiconductor device according to claim 102, wherein an output terminal of the first logical circuit is electrically connected to at least one inverter circuit.

113. (Previously Presented) A semiconductor device according to claim 103, wherein an output terminal of the first logical circuit is electrically connected to at least one inverter circuit.

114. (Previously Presented) A semiconductor device according to claim 102, wherein an output terminal of the second logical circuit is electrically connected to at least one inverter circuit.

115. (Previously Presented) A semiconductor device according to claim 103, wherein an output terminal of the second logical circuit is electrically connected to at least one inverter circuit.

116. (Original) A display device using a semiconductor device according to claim 100.

117. (Original) A display device using a semiconductor device according to claim 101.

118. (Original) A scanner using a semiconductor device according to claim 100.

119. (Original) A scanner using a semiconductor device according to claim 101.

120. (Original) A portable information terminal using a semiconductor device according to claim 100.

121. (Original) A portable information terminal using a semiconductor device according to claim 101.

122. (Previously Presented) A semiconductor device according to claim 1, wherein the first circuit comprises shift register.

123. (Previously Presented) A semiconductor device according to claim 2, wherein the first circuit comprises a shift register.

124. (Previously Presented) A semiconductor device according to claim 3, wherein the first circuit comprises a shift register.

125. (Previously Presented) A semiconductor device according to claim 4, wherein the first circuit comprises a shift register.

126. (Previously Presented) A semiconductor device according to claim 5, wherein the first circuit comprises a shift register.

127. (Previously Presented) A semiconductor device according to claim 6, wherein the first circuit comprises shift register.

128. (Canceled)

129. (Previously Presented) A semiconductor device according to claim 100, wherein the first circuit comprises a shift register.

130. (Previously Presented) A semiconductor device according to claim 101, wherein the first circuit comprises a shift register.